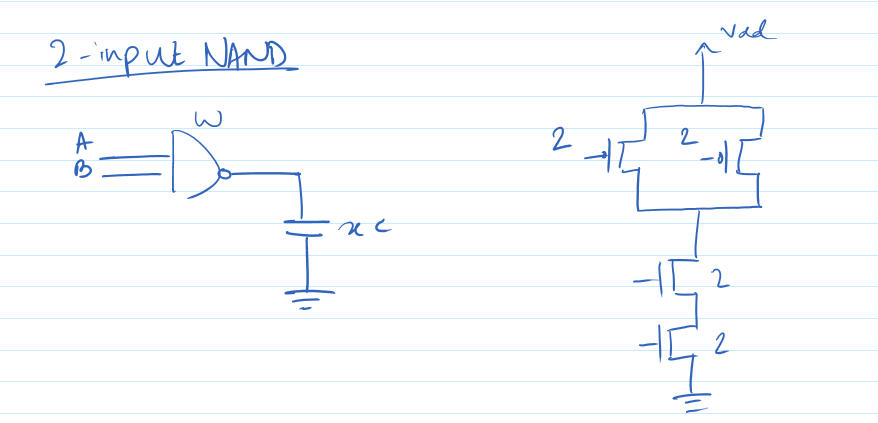
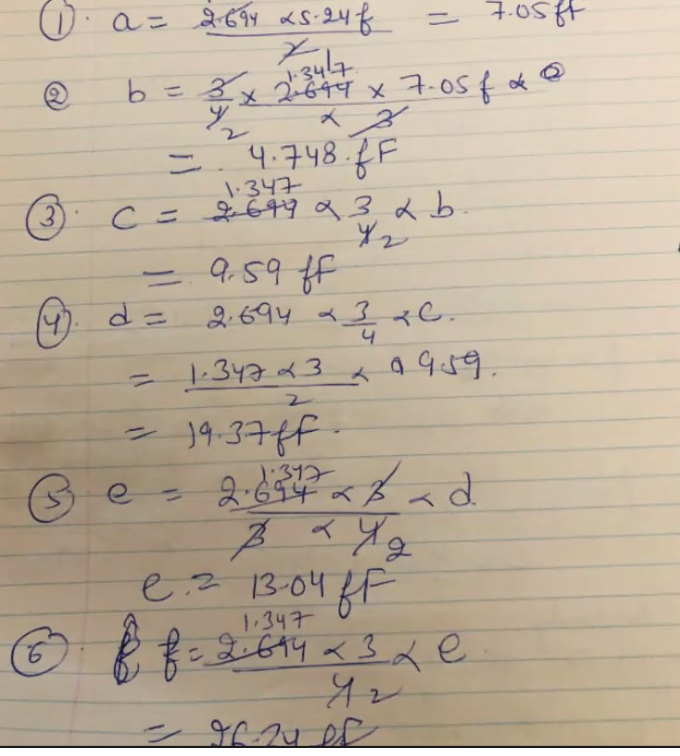
Get the sizing calculations for each nand gate in the schematic

The final size of each of the NAND gate will be ½ of the value calculated. 

Foe example, in the picture below: 

The width of a will be 7/2 = 3.5fF

**Analyses>tran>20n**

**Variables>copy form cell view>cload>72f**

**Output to be plotted (5 nets) = A B Cin SUM Cout>select on schematic**

**Netlist and run**

**Split the graphs using this** 